THE STATE UNIVERSITY OF NEW JERSEY
RUTGERS

College of Engineering
Department of Electrical and Computer Engineering

332:322 **Principles of Communications Systems** **Spring 2003**

Envelope Detection Primer

1. FIGURE 1 shows the circuit diagram of an envelope detector. It consists simply of a diode and resistor-capacitor (RC) filter. On a positive half cycle of the input signal, the diode is forward biased and the capacitor C charges up rapidly to a peak value of the input signal. When the input signal falls below this value, the diode becomes reverse biased and the capacitor discharges slowly through the load resistor R_l. The discharging process continues till the next positive half cycle. Thereafter the charging-discharging routine is continued. To answer the questions below assume that the forward resistance of the diode is r_f and bandwidth of the message signal is W.

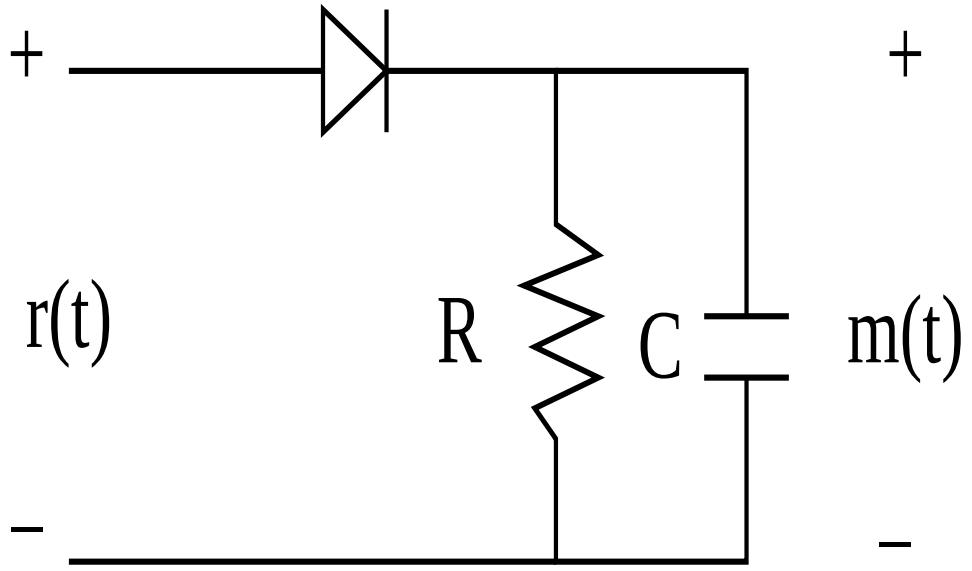

Figure 1: Envelope Detector

(a) Specify the condition that must be satisfied by the capacitor C for it to charge rapidly and thereby follow the input voltage up to a positive peak when the diode is conducting.

(b) Specify the condition which the load resistor R_l must satisfy so that the capacitor C discharges slowly between the positive peaks of the carrier wave, but not so long that the capacitor voltage will not discharge at the maximum rate of change of the modulating wave.