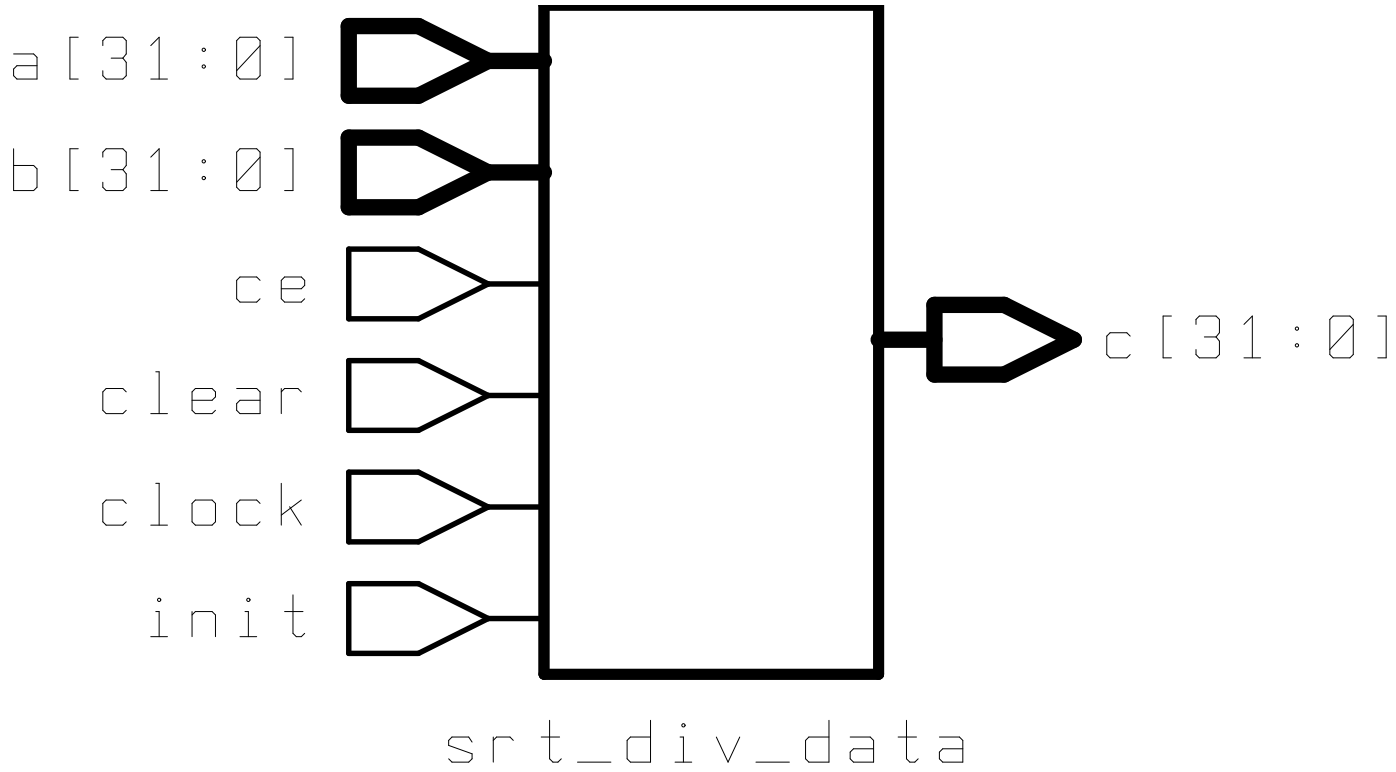
a[31:0]
b[31:0]
ce
clear
clock
init
c[31:0]
srt_div_data