Software Defined Radio Architectures for Interference Cancellation in DS-CDMA Systems

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Abstract

Third-generation (3G) wireless systems call for strategies that can improve achievable performance and data rates while providing flexibility and affordability. Software defined radio (SDR) technology is promising to provide the required flexibility in radio frequency (RF), intermediate frequency (IF) and baseband signal processing stages. Baseband signal processing techniques such as interference cancellation for direct-sequence code division multiple access (DS-CDMA) systems have the potential to provide the higher performance requirements of 3G systems. With advances in digital signal processor (DSP) technology, the gap between the complexity of interference cancellation algorithms and available processing speeds is narrowing. However, 3G system requirements are ever pushing the envelope of signal processing algorithms required including multiuser detection schemes that are considered to be attractive and viable candidates. WINLAB has been working on an attractive SDR solution, to provide flexibility and handle the processing speeds required of 3G radio receivers. The approach is based on SDR architectures that partition radio receiver processing into two core technologies (field programmable gate arrays (FPGA) and DSP devices). We present a summary of the SDR work at WINLAB that is based on using this mixed signal processing approach for implementation of nonlinear interference cancellation and linear multiuser detection algorithms.

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1 Introduction

Third generation (3G) wireless systems are being driven by the desire to support innovative broadband multimedia services. While second generation systems such as GSM, IS-136 and IS-95 are designed to carry speech and low-bit-rate data, 3G systems are expected to provide seamless wireless access to multimedia services, some of which that are not yet defined. The common theme that all variants of 3G systems adhere to is the need to provide high-bit-rates. For example, it is desired that these systems will offer at least 144 Kbps (possibly higher) for high mobility users with wide-area coverage and 2 Mbps for low-mobility users with local coverage. Additionally, multimedia traffic presents coexistence of diverse services with varied traffic characteristics. The diversity of services presented results in the need for provisioning variable quality of service (QoS) in these networks. Air interfaces in these systems will need to be able to support services with different bit-error rates, delay, and rate requirements. Direct-sequence CDMA (DS-CDMA) technology is being promoted as an air interface that holds great promise for 3G systems. Specifically, in Japan and Europe the common air interface that has been consolidated[1] is now commonly referred to as wideband CDMA (WCDMA). In the United States, the Telecommunication Industry Association has chosen a slightly different CDMA air interface that is referred to as cdma2000. Both air interfaces though require that it be backward-compatible with existing second generation interfaces.

The above standardization activities, the evolution of new services and varied QoS requirements all call for increasing the capacity of CDMA systems that are primarily limited by multiple access interference (MAI). This has prompted interest in signal processing algorithms that can mitigate interference and achieve increased capacity. Further, recent results from information theoretic considerations also show that successive interference cancelation with single-user decoding can achieve all points in the capacity region of an AWGN channel [3]. Another approach to interference mitigation is multiuser detection [4], where signals of all users in the system are jointly decoded. The significant capacity gains achieved by

[1] Japan's standardization body, the Association for Radio Industry and Business (ARIB) and the European Telecommunications Standards Institute (ETSI) each agreed on the common air interface in 1998 (see [1, 2])

such interference cancellation and multiuser detection algorithms makes them very attractive candidates for baseband receiver processing in 3G systems. These improved receivers that have been proposed over the conventional receiver have often been accompanied with an increase in complexity that has raised questions about the feasibility of these techniques for practical implementation. There is a wide range of possible performance/complexity combinations possible (see [4–6] and the references therein).

The main impediment to proving the feasibility of multiuser detection in real systems has been the disparity in processing speeds afforded by current DSP technology and that required by the detection/estimation algorithms. While the processing speeds of DSP technology is increasing quite significantly, the requirements of 3G systems are ever pushing the envelope of signal processing capabilities required. These include tasks such as (but not necessarily limited to) acquisition of high data rate signals, channel estimation for frequency selective fading channels, fast signal quality estimation algorithms to be used in power control, and optimum combining of signals for diversity gains in space and time. Customized ASIC designs for interference cancelling receivers that seem like a feasible option in the near future encounter problems of flexibility [7]. Flexibility in 3G wireless systems is desirable not only in compatibility with other systems/standards but also in terms of QoS requirements. While radio resource management algorithms (such as power control and call admission control) can provide certain levels of variability in QoS, an alternate approach is to use reconfigurable radio architectures to provide diverse QoS guarantees. Ideally, a combination of receiver flexibility and integrated radio resource management may offer the widest range of QoS guarantees. At WINLAB, we have been addressing the issues of both signal processing complexity and reconfigurability through a software-defined-radio (SDR) testbed for interference cancellation.

Software defined radios were historically considered as candidates for military applications where the focus was on the flexibility to communicate over several different radio frequency (RF) bands and possibly different air interfaces. With the recent interest in commercialization of software radios for 3G systems [8], the term SDR has now come to stand for more than just that. While compatibility between standards is still attractive, SDRs are shaping to be software and hardware reconfigurable radios in the RF, IF as well as baseband processing stages [9–12]. The wide range of wireless system components that require this flexibility ranges from multimode multiband handsets to reconfigurable base stations. Our work on SDR at WINLAB has been to date primarily on baseband signal processing architectures for use at the base station. WINLAB has been developing implementation proofs for nonlinear interference cancellation and linear multiuser detection via a signal processing dichotomy into two core technologies, FPGA and DSP devices [12–15]. The attractiveness of this approach is that it simultaneously handles the complexity issue of signal processing algorithms as well as the dynamic reconfiguration of receivers to achieve variable QoS requirements.

2 Interference Mitigation Algorithms

While it may seem that the partitioning of functionality leads to rigid architectures, it is possible to achieve dynamic reconfigurability amongst a wide class of interference cancellation schemes [12,14,15]. We consider the implementation of the following receivers using the mixed FPGA and DSP approach: (1) the matched filter receiver (MF), (2) the successive interference canceller (SIC) [16], (3) the approximate decorrelator (AD) [17], (4) the exact decorrelator(DC) [18] and (5) the minimum mean-squared-error detector(MMSE) [19]. Using a "modified" matched filter approach, dynamic reconfigurability amongst these receiver structures can be achieved via a software radio implementation.

For simplicity in illustration, consider the case of synchronous reception of K users in a system. In this case, the output of the matched filter for the k^{th} user can be written as

$$y_k = A_k b_k + \sum_{j \neq k} A_j b_j \rho_{jk} + n_k, \;\; k = 1, \cdots .K \tag{1}$$

where A_k, and $b_k \in \{-1, 1\}$, are the amplitude and the bit of the k^{th} user respectively, and $n_k = \sigma \int_0^T n(t) s_k(t) dt$, with $s_k(t)$ being the signature waveform of the k^{th} user which is assumed to have unit energy. The crosscorrelation between the signature waveforms is defined as

$$\rho_{jk} = \int_0^T s_j(t) s_k(t) dt. \tag{2}$$

Let $\mathbf{R}$, the matrix of crosscorrelations among the user pairs be such that its ij^{th} entry is ρ_{ij}, and let $\mathbf{A} = \mathrm{diag}\{A_1 \cdots A_K\}$ be a diagonal matrix of the users' amplitudes. In this case, linear detectors corresponding to MF, DC, AD and MMSE can be easily realized for the k^{th} user by correlating the incoming signal with a "modified" filter $h_k(t)$ (see [12, 14]). Specifically, the decorrelator is realized as

$$h_k(t) = \sum_{j=1}^{K} \mathbf{R^{+}_{kj}} s_j(t), \tag{3}$$

where $\mathbf{R^{+}_{kj}}$ denotes $(\mathbf{R^{-1}})_{kj}$. The approximate decorrelator can be realized as

$$h_k(t) = s_k(t) - \sum_{j \neq k} \rho_{jk} s_j(t), \tag{4}$$

and the MMSE detector as

$$h_k(t) = \sum_{j=1}^{K} (\mathbf{R} + \sigma^{\mathbf{2}} \mathbf{W^{-1}})^{+}_{\mathbf{kj}} s_j(t), \tag{5}$$

where $(\mathbf{R} + \sigma^{\mathbf{2}} \mathbf{W^{-1}})^{+}_{\mathbf{kj}}$ denotes $[(\mathbf{R} + \sigma^2 \mathbf{W^{-1}})^{-1}]_{kj}$, with $\mathbf{W} = \mathbf{A}^{\top}\mathbf{A}$. Note that for the matched filter $h_k(t) = s_k(t)$.

The SIC scheme is based on the algorithm [16] illustrated in Figure 1. The basic operations of the SIC algorithm are (i) detect one user with the conventional detector, (ii) regenerate the baseband signal for this user, and (iii) cancel the regenerated signal from the received baseband signal. Then this operation is repeated for successive users. The idea behind the SIC is that successive cancellations result in reduced multiple access interference (MAI) for the remaining users. To obtain best results, the strongest user should be cancelled first followed by the second strongest and so forth. Thus the SIC algorithm implicitly requires a reordering of users (based on received signal powers) for best results.

The received signal $r_k(t)$, after stage k of the cancellation is given by:

$$r_k(t) = r_{k-1}(t) - A_{k-1} \hat{b}_{k-1} s_{k-1}(t), \tag{6}$$

where $r_{k-1}(t)$ is the received signal at stage $k-1$ and $\hat{b}_{k-1}$ is the corresponding estimate of the bit decision. Using the above recursion, it can be easily shown that the SIC algorithm can be written as matched filtering through a bank of K receivers whose outputs are:

$$y_1^{SIC} \quad = \quad y_1$$

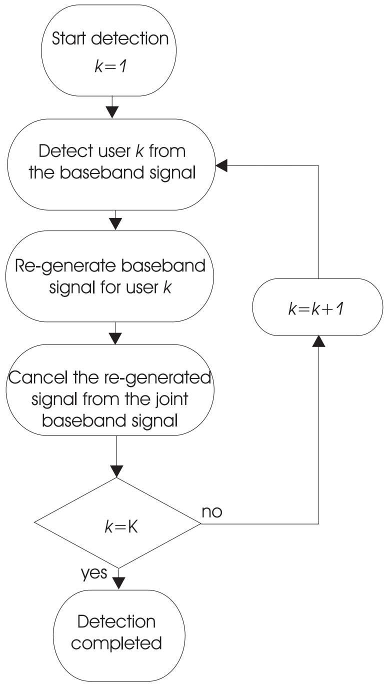


Figure 1: Flow chart of SIC scheme

$$\begin{aligned}
y_2^{SIC} &= y_2 - A_1\hat{b}_1\rho_{1,2} \\
y_3^{SIC} &= y_3 - A_1\hat{b}_1\rho_{1,3} - A_2\hat{b}_2\rho_{2,3} \\
&\vdots \\
y_K^{SIC} &= y_K - \sum_{i=1}^{K-1} A_i\hat{b}_i\rho_{i,K}
\end{aligned} \tag{7}$$

The above implementation of the SIC algorithm is nonlinear in that it uses hard decisions in successive stages and we refer to this as nonlinear successive interference cancellation (NSIC). It is possible to realize a "modified" matched filter structure for the SIC [15], by replacing the bit estimates in the above set of equations with the true bit values. This results in a linear successive interference cancellation (LSIC) scheme where the set of equations in (7) in vector form are

$$\mathbf{y}^{\mathbf{SIC}} = (\mathbf{R}^{\mathbf{L}}\mathbf{A})^{-\mathbf{1}}\mathbf{y}, \tag{8}$$

where $\mathbf{y}^{\mathbf{SIC}} = [y_1^{SIC} \cdots y_K^{SIC}]^\top$, and $\mathbf{R}^{\mathbf{L}}$ is a lower triangular cross-correlation matrix obtained from $\mathbf{R}$ by setting the elements above its main diagonal to zero. Then it follows that the SIC can be realized for the k^{th} user (in the cancellation order) as a modified matched filter given as

$$h_k(t) = \sum_{j=1}^{K} (\mathbf{R^L A})^{+}_{\mathbf{kj}} s_j(t), \tag{9}$$

where $(\mathbf{R^L A})^{+}_{\mathbf{kj}}$ denotes $((\mathbf{R^L A})^{\mathbf{-1}})_{kj}$. The reason for implementing the LSIC algorithm is that it facilitates reconfigurability [15]. In other words, the MF, AD, DC, MMSE and LSIC receivers can all be implemented as appropriate modified matched filters or single-user receivers for multiuser systems.

3 SDR Architecture for Interference Cancellation

Figures 2 and 3 show the canonical SDR architecture for reconfigurable linear detection and nonlinear interference cancellation, respectively. The architecture includes channel processing (such as translation from IF to baseband), environment processing (e.g., estimation of signal and interference parameters and correlations), matched filtering and information bit-stream processing (e.g., FEC or convolutional decoding, soft decisions etc.). These functionalities are partitioned into FPGA and DSP devices according to processing speed requirements. The SDR architecture for linear detection is designed to dynamically reconfigure the (modified) matched filter according to the desired QoS (corresponding to the one of the appropriate linear detectors) [12]. The SDR architecture for nonlinear successive interference cancellation (NSIC) is designed to streamline the operation of successive cancellations among users [13].

The core of the hardware part of the SDR testbed at WINLAB (see Figure 4) is based around APTIX MP3 board [20] with up to 12 FPGA components (up to 432,000 programmable gates) for sample-level processing tasks with rates of up to 30.0 MHz. Information-rate tasks (Viterbi decoding, deinterleaving etc.) are performed by the VME-bus based Pentek 4270 Quad TMS320C40 floating point DSP Processor board [21]. For fixed point implementations, a Pentek 4290 Quad TMS320C6201 fixed point DSP Processor board is used. As a baseband front-end, the testbed has two sets of dual (I and Q) analog-to-digital converters for input (Analog Devices AD9762XR 12-bit, 41 MHz convert-

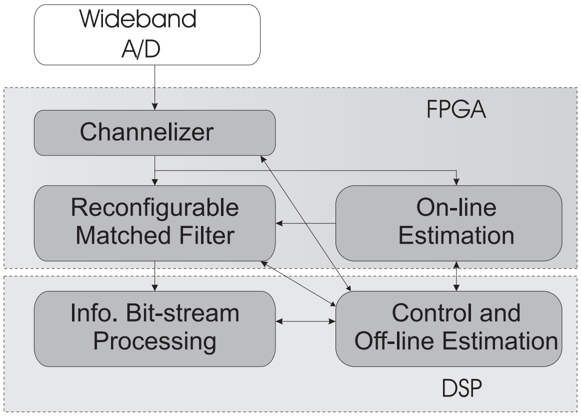


Figure 2: Functional Architecture of SDR for Reconfigurable Linear Detection

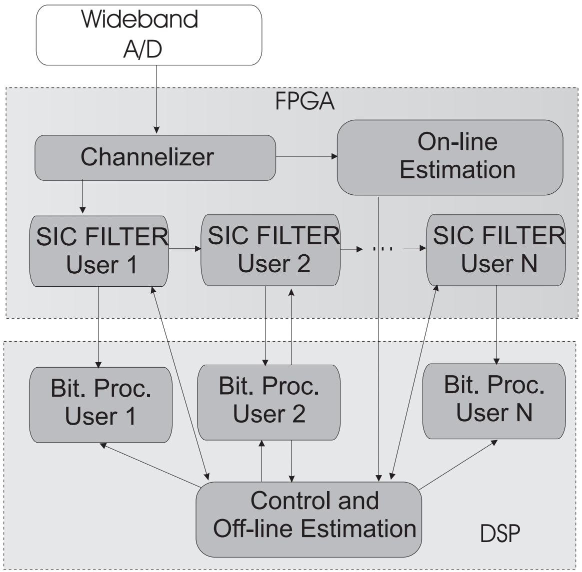


Figure 3: Functional Architecture of SDR for Nonlinear Interference Cancellation

ers [22] and PENTEK 6472 10-bit, 70 MHz converters [23]) and one set of digital-to-analog converters (Analog Devices AD9042ST 12-bit, 100 MHz [24]). Analog Devices converters are connected to the FPGA board through the custom adapters while PENTEK converters are connected to the DSP via a Multiband Digital Receiver (PENTEK 4272) [25] acting as a *channelizer* in Figures 2 and 3. In addition, the fixed point DSP board has a separate Dual Wideband Digital Receiver and A/D converter board (PENTEK 6216). The channelizer performs frequency down-conversion, low-pass filtering and decimation of the sampled baseband signal. It is used for selection of the service bandwidth (i.e., the *tuning band*) from among those available in the sampled signal. The Multiband Digital Receiver used as a channelizer has two narrowband receivers with dynamic range of $1KHz - 1MHz$ and one wideband receiver with dynamic range of $2MHz - 35MHz$. Thus it is capable of supporting a wide range of output sample rates. The Wideband Digital Receiver features two channels with input bandwidths of up to $30MHz$.

3.1 Logical Partitioning of the Architecture

Figure 5 shows the necessary operations required by each type of detector among the MF, LSIC, NSIC, AD, DC and MMSE receivers. All of the above receivers require two common generic operations namely, estimation of path delays of the users and the generation of PN sequences $\{s_k(t)\}$ of the users in the system. The MF is probably the simplest in that for any user k, it just uses the information from these two generic operations in determining the timing offset of the PN sequence $s_k(t)$ for the specific user. For the AD, the complexity is slightly higher than that of the MF in that the "modified" matched filter taps are adjusted according to the formulation in equation (4). As seen in Figure 5, the additional functionality required here is the crosscorrelation values $\{\rho_{kj}\}$ and also the signature sequences of all the users $\{s_k(t)\}$. For the LSIC receiver, the complexity involves ordering of users according to received power strengths followed by a computation of the lower triangular matrix $\mathbf{R_L}$ and then subsequent inversion of the matrix $\mathbf{R^L A}$ (see equation (9)). From (3), we see that the functional operations required for the DC are additionally the computation of the inverse matrix of crosscorrelations $\mathbf{R^{-1}}$ and also the column vector

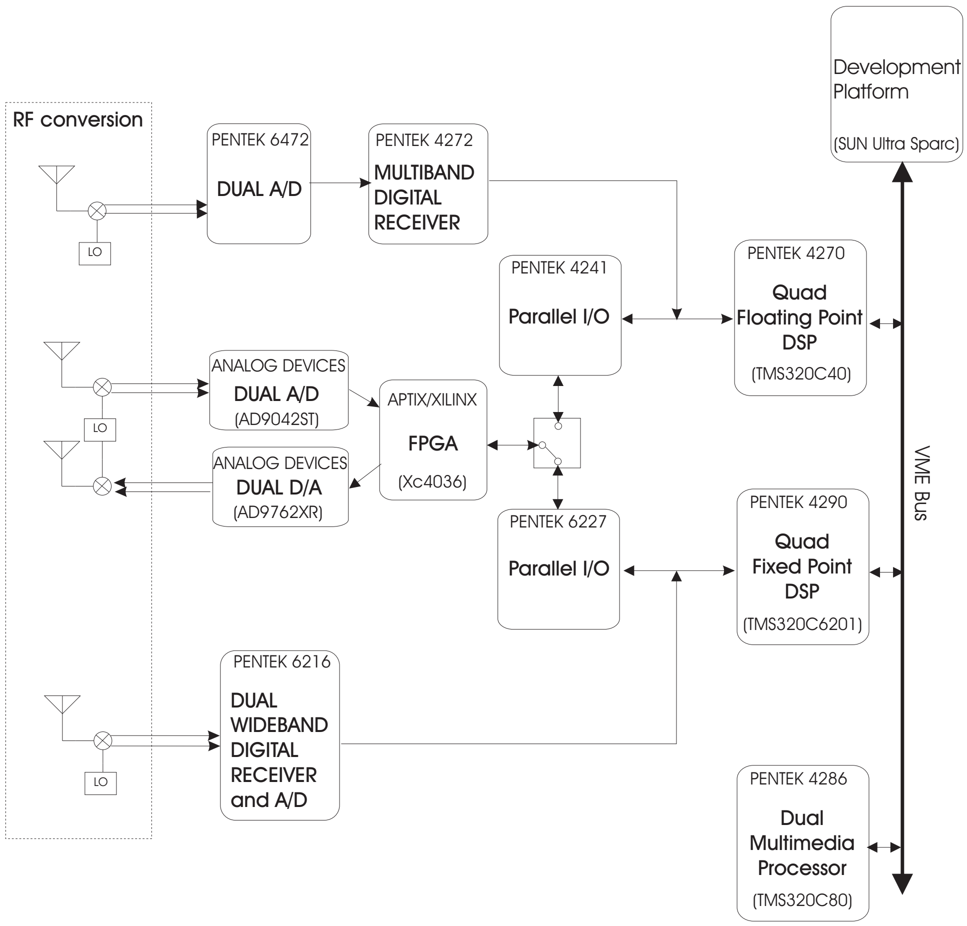


Figure 4: Testbed block diagram

corresponding to the k^{th} user, i.e., $\mathbf{R}^{+}_{\mathbf{kj}}$. The MMSE receiver (see equation (5)) incurs the additional complexity over the DC in that it also requires estimates of the received signal powers of the users in the system.

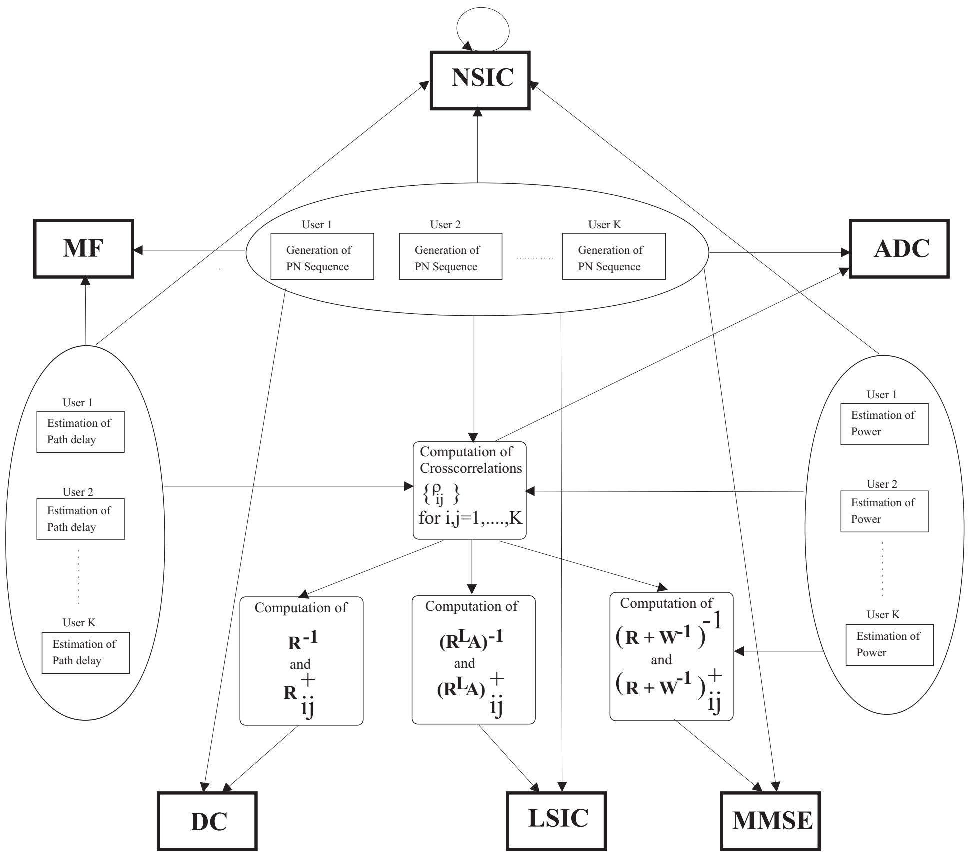


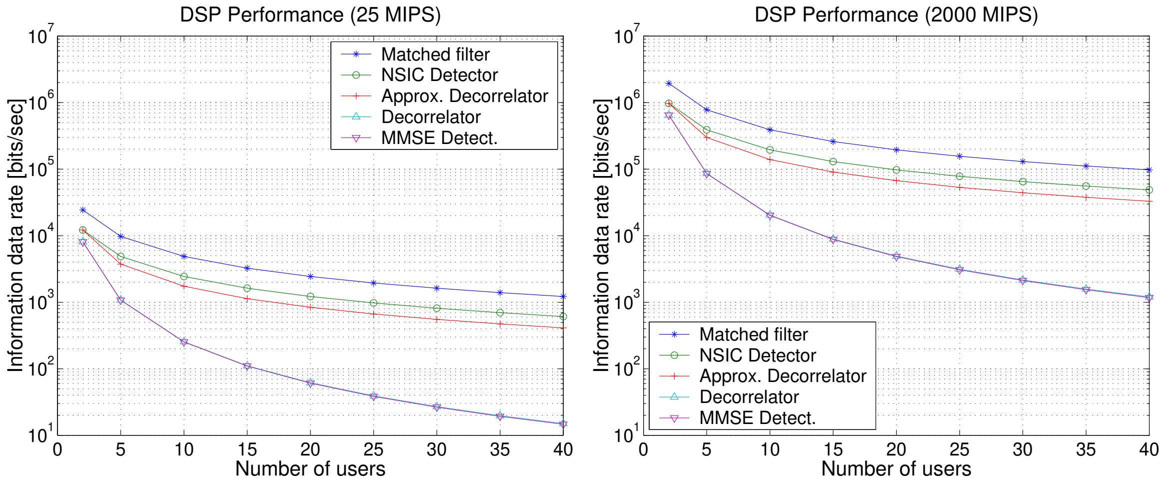
Figure 5: Logical Partitioning of Functionality in a SDR for Interference Cancellation

For the NSIC receiver, the relevant operations include estimation of path delays of the users, the generation of PN sequences and amplitude (power) estimates. This information is needed in order to regenerate the baseband signal before cancellation in successive stages. The amplitude estimates could be obtained from the linear correlator output of the conventional detector. This has been shown to be a sufficiently good estimate, even though better estimates can be obtained by using more advanced signal processing algorithms or even simple averaging over symbols. We do not explicitly address the issue of estimating the path delays or the received signal powers of the users in the system. However, the SDR architecture presented here is versatile in that it can easily allow a variety of signal processing algorithms to be implemented for accomplishing the required estimation. The detection and cancellation procedure is repeated until as many users need to be cancelled using the SIC scheme. The remaining users are then demodulated by a bank of conventional detectors. The users need to be ranked in the order of received powers before initiating the cancellation. Power control can be integrated with NSIC to obtain potential reductions in inter-cell interference [13]. Furthermore, the requirement of strict ranking of users before cancellation can be relaxed. The order of cancellation would be constant over a longer period of time, since the power of the individual users are controlled. This leads to a low reordering rate of users which is desirable for a hardware implementation of the NSIC detector.

3.2 All DSP Implementation

The rapid progress in DSP technology has resulted in the creation of high-speed DSPs, power-managed DSP chips, and programmable DSPs. With the continued evolution to higher speeds in the near future, it is conceivable that an all DSP implementation may be possible for the SDR architecture for interference cancellation. However, the complexity of the signal processing algorithms for interference cancellation is quite significant, that there is still a gap between the available DSP speeds and that required algorithm speeds. As an illustration, the achievable data rates are shown in Figure 6 for the different receivers for a system with a processing gain of 128 and an oversampling factor of 4. The active constraint in the examples shown is the processing speed of the DSP device used. The total number of users that can be supported under each receiver is shown for both a DSP device capable of 25 MIPS and the more recent one that can handle 2000 MIPS. It is seen that the the improvement is quite significant with the faster DSP, but still is well below expectations of 3G systems. We see that an all DSP implementation imposes serious constraints on the achievable data rates when the number of users increases.

The receiver designs considered in the above illustration do not explicitly take into account the processing requirements due to estimating parameters such as timing information,



(a) TMS320C40 DSP

(b) TMS320C6201

Figure 6: Achievable Rates vs. Number of Users

multipath channel response, and received power levels. The solutions being proposed for WCDMA systems include coherent detection on the reverse link with multistage successive interference cancellation for multirate systems [26]. The feasibility of the above concept requires fast algorithms for recursive channel estimation [27, 28], fast cell search for asynchronous operation and coherent spreading-code tracking [29], fast transmit power control on both reverse and forward link [26, 30]. In addition, antenna diversity is also being considered in conjunction with some of the above algorithms. Clearly these signal processing algorithms are very high in sophistication and complexity, and only increase the demands on DSP speeds required. The signal processing dichotomy in the SDR architecture into FPGA and DSP devices is a natural fit that alleviates some of the above concerns.

3.3 Resource Partitioning of the Architecture

3.3.1 Reconfigurable Linear Detection

The reconfigurability of linear multiuser receivers allows for the integration of multimedia services over wireless channels with variable quality of service (QoS) requirements. While radio resource management algorithms can provide certain levels of variability in QoS guarantees, reconfigurable radio architectures can also provide diverse QoS guarantees ranging in several orders of magnitudes in terms of BER requirements [12].

The SDR architecture for reconfigurable linear detection is implemented by partitioning the resources between FPGAs and DSPs as shown in Figure 7. The FPGA segment of the architecture includes the PN sequence generators, two reconfigurable blocks (that determine the filter taps of the appropriate linear receivers), an on-line estimator module and the correlator. The motivation for the particular selection of constituents that comprise the FPGA segment is that the functionality provided by each constituent here can be easily handled by the processing speeds of the FPGA hardware. The two reconfigurable blocks contain the core of the sample level processing for each of the detectors and are actually implemented in separate FPGA components to facilitate on-the-fly reconfigurability[2]. This particular partitioning enables us to reconfigure one of the blocks while the other is running and therefore, by oversizing the hardware, avoid loss of data during switchover to different receiver structures (see [14]). The rest of the sample level processing logic (PN sequence generators, control multiplexer, and correlator) is implemented in a separate FPGA component since it does not require reprogrammability. The on-line estimation block is used to perform timing estimates of the incoming signals which are then fed along with the reference PN sequences to compute the appropriate filter taps. Further, there is also a provision for refining the on-line estimates by using more sophisticated off-line algorithms. Additionally, an FPGA component is used as an interface between the DSP segment and APTIX board [20].

The more algorithmically complex operations required are implemented in the DSP segment of the SDR architecture shown in Figure 7. This segment is implemented using a a quad TMS320C40 DSP board. The operations performed in this segment include off-line estimation procedures, information bit-stream processing as well as control and reconfiguration management. The off-line estimation block includes estimation of powers of the received signals (for the MMSE detector), and computation of the inverse of the matrix of crosscorrelations(in the case of both the decorrelator and the MMSE detector). Further,

[2]The above duplicity may be avoided in the XC62xx XILINX FPGA family which has in-system reprogrammability allowing sections of the device to be reprogrammed without disturbing circuits running in other sections

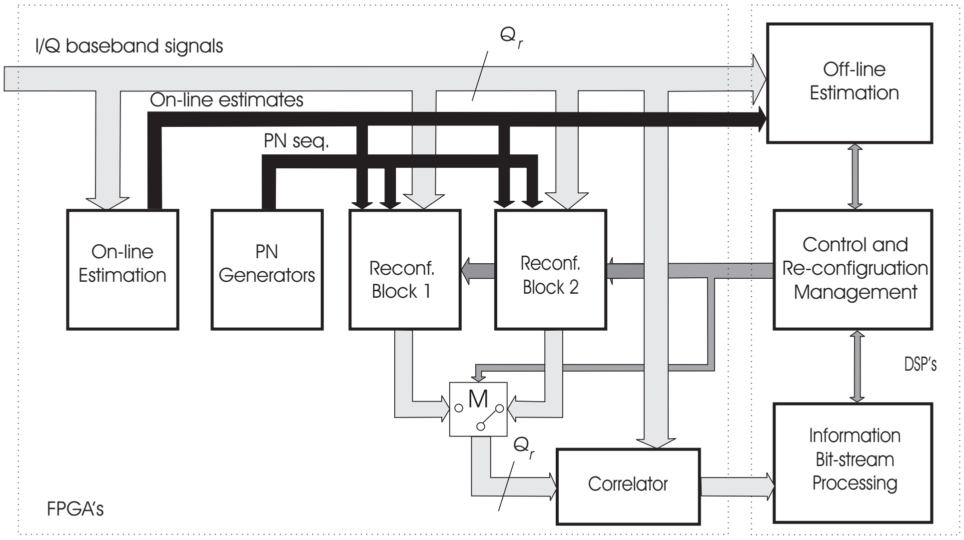


Figure 7: SDR Implementation for Reconfigurable Linear Detection

it can also refine estimates of the on-line estimation block in the FPGA segment. The information bit-stream processing functions performed vary from error control techniques, such as FEC or convolutional decoding, to soft decision decoding.

The control and reconfiguration management block in the DSP segment of the architecture basically determines the variable QoS that can be achieved by dynamic reconfiguration of the receiver structures in the FPGA segment. The reconfiguration of the blocks in the FPGA segment is directly controlled by the control and reconfiguration management block. The subsequent switching amongst receivers is achieved by a control multiplexer M (shown in Figure 7) that is also controlled by the control and reconfiguration management block. Thus the DSP segment of the device acts to achieve the variable QoS requirements of the specific type of service. Implicit in the control and reconfiguration management block is also the notion of sensing the QoS demand of a specific data stream and also the actions that encompass environment processing such as sensing interference levels. The reader should note that the DSP devices have access to the configuration bit-streams for each of the receiver structures and can download the particular configuration bit-stream as and when required.

3.3.2 Nonlinear Interference Cancellation

Nonlinear successive interference cancellation schemes [16, 31, 32] are attractive from an implementation point of view in that they can perform sequential replica generation and subtraction of MAI. The potential drawback of these algorithms is that they require extremely accurate channel estimates for regeneration and subtraction. Further, the ranking of users according to received signal strengths requires accurate power estimates. In the absence of accurate channel and power estimates, these algorithms are susceptible to degradation in performance due to error propagation. However, the potential gains that can be had from accurate implementations [3, 33] make these worthwhile candidates for 3G systems [34].

The SDR architecture for NSIC [13] is implemented by partitioning the resources between FPGAs and DSPs as shown in Figure 8. Although the NSIC gain is non-trivial and worth pursuing, a requirement for very low complexity still exists. The approach taken in [13] was to view the NSIC scheme as an extension to the existing conventional detector, thus minimizing the number of modifications. Owing to the issue of backward compatibility to second generation systems, it is desirable for the NSIC implementation that it be possible (if necessary) to support the same bit rate and modulation scheme as the conventional detector. The choice of implementation in [13] was a *pipelined structure* shown in Figure 8 for implementing the NSIC scheme.

The structure consists of a chain of interference cancelling (SIC) filters. Each of these filters is adaptively detecting and cancelling a specific user from its input signal. The filter is matched to a user corresponding to the applied PN sequences (`PNI` and `PNQ` in Fig. 8) and estimated path delays (`TAU` in Fig. 8). The output of the SIC filter is essentially the same as the input signal but with the current user cancelled. It is seen that each SIC filter operates on both an I and Q baseband branch due to non-coherent reception (as in IS-95). From the description of the NSIC scheme it should be recalled that the first SIC filter should be matched to the strongest user and so forth.

As the NSIC scheme with symbol averaging is based on hard decisions, a symbol estimate is necessary before the corresponding user can be cancelled. This implies that each

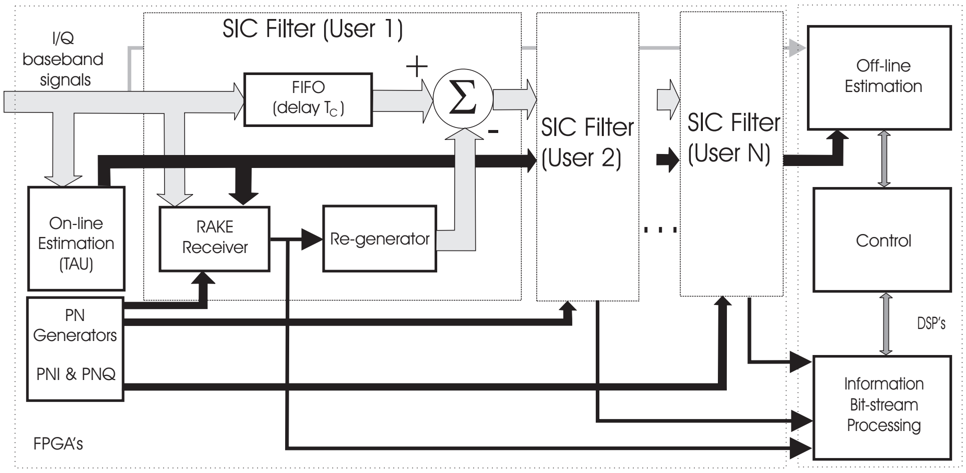


Figure 8: SDR Implementation for Nonlinear Interference Cancellation

SIC filter must complete its correlation before it can initiate the cancellation. This introduces a delay through each SIC filter denoted by T_c. This delay corresponds to the symbol time plus the multipath delay spread because all multipath signals must be received before a reliable estimate can be made. It is seen that the I and Q input signals are passed to a RAKE receiver. The RAKE receiver is responsible for performing the multipath combining and estimating the transmitted symbol. The symbol estimate and the correlator output specifying the amplitude of the user are next used by the *regenerator* to recreate the I and Q baseband signals of the current user. The detection of a symbol has a duration of T_c before sample-by-sample subtraction can be initiated with the regenerated signals. For delaying the input signals a FIFO buffer is used as shown in Fig. 8. From a complexity point of view it is convenient to have a fixed delay in the FIFO buffers since variable delays are more difficult to implement in hardware. A fixed delay is obtained by setting T_c equal to the symbol time plus the maximum expected delay spread of the channel.

From considering the pipelined structure it is seen that each SIC filter is operating independently of the other SIC filters and both synchronous and asynchronous transmission are supported by the structure. All filters are operating simultaneously leading to full utilization of the hardware. By introducing the detection delay, the processing time requirements to the RAKE receivers remain unchanged. With the regenerator implemented in real-time, the proposed structure can support the same bit rate as the conventional detector. However, the increased detection delay may set a limit on how many cancellations can be performed. As the symbol rate increases this potential limitation is relaxed.

A disadvantage of the pipelined structure appears when considering the dynamic features. As mentioned earlier the performance of the SIC scheme is based on cancelling the strongest users first. However, with the pipelined structure it is difficult to reorder users as the SIC filters are operating on samples with different delays. To illustrate this, consider what happens if the weakest user suddenly becomes the strongest user. This user should then be moved up in front of the filter chain. If this is done instantaneously all the samples stored in the SIC filters located in between would be lost. By using a power control scheme in conjunction with cancellation [13], the power ranking is greatly stabilized and the re-ordering rate is reduced. The regeneration process contains a set of parallel multiplications and additions. The desired simplicity and the static behavior of the regenerator further suggest an implementation in dedicated hardware.

3.4 Hardware Complexity

In Table 1, we show the relative hardware complexity[3] of the different cancellation schemes in terms of the required number of configurable logic blocks (CLB). A CLB, in case of XILINX 4000 series FPGA, comprises of a pair of flip-flops and two independent (Boolean) logical four-input function generators [35]. As can be seen the complexity for each detector increases with both increasing number of users K and increasing precision in quantization (Q_r denotes the number of bits used in quantization). As expected, the matched filter complexity remains invariant to the number of users in the system and depends only on the precision of quantization.

Even though the decorrelator (and the MMSE) achieves better QoS, it comes at the expense of an exponential increase in complexity (with increasing number of users) over the SIC[4] and AD detectors. This directly maps to an increase in processing power requirements of the FPGA segment of the SDR architecture. Switching to lower order receivers when the

[3]The complexity estimates for NSIC given in Table 1 are based on implementation described in [13] which has much lower complexity than LSIC, the modified matched filter based implementation (which has the same complexity as DC and MMSE detectors).

[4]Note that the SIC receiver requires explicit ordering of users according to their relative received powers. This is not accounted for in the Table 1

Quantization	MF	NSIC	AD	LSIC, DC & MMSE
$Q_r = 4$ bits	25	36	$31 + 13K$	$37 + 3K(K-1)$
$Q_r = 5$ bits	27	44	$40 + 14K$	$47 + \lceil 13/4 \rceil K(K-1)$
$Q_r = 6$ bits	29	57	$57 + 15K$	$64 + \lceil 7/2 \rceil K(K-1)$

Table 1: Complexity comparison of different detectors (in number of CLB's for each user)

QoS requirements are moderate has been considered in [14]. The complexity of operations required to be performed in the DSP segment of the architecture involve matrix inversion and off-line estimation of amplitudes. The complexity trade-offs for linear multiuser schemes in terms of add-multiply floating point operations can be found in [12, 36].

4 Conclusions and Future Directions

Provisioning of services in third generation wireless systems require flexible and versatile air interfaces. SDR architectures promise to bring this capability for 3G systems such as WCDMA by making possible implementation of sophisticated interference mitigation algorithms. Our studies at WINLAB on the feasibility of such a concept shows that it is possible to achieve the flexibility and versatility required of air interfaces by using a combination of DSP with a reconfigurable hardware processing subsystem. The key idea is to enable the offload into hardware of processing (speed) intensive operations. Achieving the appropriate choice of digital architecture is a trade-off between power consumption, flexibility in performance, and cost. Experimental results on the performance and reconfigurability of the SDR architecture at WINLAB show that diverse services can be simultaneously supported by flexible radio interface design. The success of nonlinear interference cancellation schemes requires accurate channel estimation and ordering of users according to relative received signal strengths. Future work will include studying the feasibility and constraints of implementing sophisticated estimation algorithms for use in conjunction with the detectors. Also of great interest is the implementation study of blind adaptive multiuser detectors such as for use in unlicensed bands.

References

[1] F. Adachi, M. Sawahashi, and H. Suda, "Wideband DS-CDMA for Next-Generation Mobile Communication Systems", *IEEE Communications Magazine*, vol. 36, no. 9, pp. 56–68, September 1998.

[2] T. Ojanpera and R. Prasad, "An Overview of Third-Generation Wireless Personal Communications: A European Perspective", *IEEE Perosnal Communications*, vol. 5, no. 6, pp. 59–65, December 1998.

[3] B. Rimoldi and R. Urbanke, "A Rate-Splitting Approach to the Gaussian Multiple-Access Channels", *IEEE Transactions On Information Theory*, vol. 42, no. 2, pp. 364–375, March 1996.

[4] S. Verdú, *Multiuser Detection*, Cambridge University Press, New York, 1998.

[5] A. Duel-Hallen, J. Holtzman, and Z. Zvonar, "Multiuser Detection for CDMA Systems ", *IEEE Personal Communications*, pp. 46–58, April 1995.

[6] S. Moshavi, "Multiuser Detection for DS-CDMA Communications", *IEEE Communications Magazine*, pp. 124–136, October 1996.

[7] M. Cummings and S. Haruyama, "FPGA in the Software Radio", *IEEE Communications Magazine*, vol. 37, no. 2, pp. 108–112, February 1999.

[8] J. Mitola, "Technical Challenges in the Globalization of the Software Radio", *IEEE Communications Magazine*, vol. 37, no. 2, pp. 84–89, February 1999.

[9] H. Tsurumi and Y. Suzuki, "Broadband RF Stage Architecture for Software-Defined Radio in Handheld Terminal Applications", *IEEE Communications Magazine*, vol. 37, no. 2, pp. 90–95, February 1999.

[10] R. H. Walden, "Performance Trends of Analog-to-Digital Converters", *IEEE Communications Magazine*, vol. 37, no. 2, pp. 96–101, February 1999.

[11] D. B. Chester, "Digital IF Filter technology for 3G Systems: An Introduction", *IEEE Communications Magazine*, vol. 37, no. 2, pp. 102–107, February 1999.

[12] I. Seskar and N. B. Mandayam, "A Software Radio Architecture for Linear Multiuser Detection", *IEEE JSAC–Special Issue on Multimedia Network Radios*, May 1999, To Appear.

[13] K. Pedersen, T. Kolding, I. Seskar, and J. Holtzman, "Practical Implementation of Successive Interference Cancellation in DS/CDMA Systems", in *Proceedings of ICUPC'96*, September 1996, pp. 321–325, Cambridge, MA.

[14] I. Seskar and N. B. Mandayam, "A Software Radio Architecture for Linear Multiuser Detection", in *Proceedings of CISS'98*, March 1998, Princeton, NJ.

[15] I. Seskar, N. B. Mandayam, and P. Hatrack, "Reconfigurable Testbed for Interference Cancellation in DS-CDMA Systems", *International Journal of Wireless Networks*, 1999, To Appear.

[16] P. Patel and J. M. Holtzman, "Analysis of a Simple Successive Interference Cancellation Scheme in DS/CDMA System", *IEEE JSAC*, vol. 12, no. 5, pp. 796 –807, June 1994.

[17] N. B. Mandayam and S. Verdú, "Analysis of an Approximate Decorrelating Detector", *Journal of Wireless Personal Communications*, vol. 6, pp. 97–111, January 1998.

[18] L. Lupas and S. Verdú, "Linear Multiuser Detectors for Synchronous Code-Division Multiple-Access Channels", *IEEE Transactions On Information Theory*, vol. 35, no. 1, pp. 123–136, January 1989.

[19] U. Madhow and M. Honig, "MMSE Interference Suppression of Direct-Sequence Spread-Spectrum CDMA", *IEEE Transactions On Communications*, vol. 42, no. 12, pp. 3178–3188, December 1994.

[20] Aptix Corporation, *FPCB Development System documentation*, 1993.

[21] PENTEK, Inc, *Operating Manual: MODEL 4270 Quad TMS320C40 DSP Board*, 1995.

[22] Analog Devices, Inc., *Data Sheet: AD9762* 12-bit, 100 MSPS+ TxDAC D/A Converter*, 1996.

[23] PENTEK, Inc, *Operating Manual: MODEL 6472 Dual Channel, 70 MHz, 10-bit, A/D Converter*, 1996.

[24] Analog Devices, Inc., *Data Sheet: AD9042 12-bit, 41 MSPS Monolithic A/D Converter*, 1996.

[25] PENTEK, Inc, *Operating Manual: MODEL 4272 Multiband Digital Receiver*, 1996.

[26] F. Adachi and M. Sawahashi, "Wideband Wireless Access based on DS-CDMA", *IEICE Transactions COM*, vol. E81-B, no. 7, pp. 1305–1316, July 1998.

[27] M. Sawahashi, Y. Miki, H. Andoh, and K. Higuchi, "Pilot Symbol-Assisted Coherent Multistage Interference Canceller Using Recursive Channel Estimation for DS-CDMA Mobile Radio", *IEICE Transactions*, vol. E79-B, no. 9, pp. 1262–1270, September 1996.

[28] M. Sawahashi, H. Andoh, and K. Higuchi, "Interference Rejection Weight Control for Pilot Symbol-Assisted Coherent Multistage Interference Canceller Using Recursive Channel Estimation for DS-CDMA Mobile Radio", *IEICE Transactions Fundamentals*, vol. E81-A, no. 5, pp. 957–972, May 1998.

[29] K. Higuchi, M. Sawahashi, and F. Adachi, "Fast Cell Search Algorithm in Inter-Cell Asynchronous DS-CDMA Mobile Radio", *IEICE Transactionson COM*, vol. E81-B, no. 7, pp. 1527–1534, July 1998.

[30] S. Seo, T. Dohi, and F. Adachi, "SIR-Based Transmit Power Control of Reverse Link for Coeherent DS-CDMA Mobile Radio", *IEICE Transactionson COM*, vol. E81-B, no. 7, pp. 1508–1516, July 1998.

[31] M. K. Varanasi and B. Aazhang, "Multistage Detection in Asynchronous Code-Division Multiple-Access Communications", *IEEE Transactions On Communications*, vol. 38, no. 4, pp. 509–519, April 1990.

[32] Y. C. Yoon, R. Kohno, and H. Imai, "A Spread-Spectrum Multi-Access System with Co-Channel Interference Cancellation for Multipath Fading Channels", *IEEE JSAC*, vol. 11, no. 7, pp. 1067–1075, September 1993.

[33] M. K. Varanasi and B. Aazhang, "Near-Optimum Detection in Synchronous Code-Divisions Multiple-Access Systems", *IEEE Transactions On Communications*, vol. 39, pp. 725–736, May 1991.

[34] M. Sawahashi, H. Andoh, K. Higuchi, and F. Adachi, "Experiments on Coherent Multistage Interference Canceller for DS-CDMA Mobile Radio", in *Proceedings of PIMRC*, September 1998, Boston, MA.

[35] XILINX, *XACT Reference Guide*, 1994.

[36] R. M. Buehrer, S. N. Correal, and B. D. Woerner, "A comparison of multiuser receivers for cellular cdma", in *Proc. of 1996 IEEE Global Telecommunications Conference*, November 1996, pp. 1571 – 1577, London, U.K.