32nm Low Standby Power NMOS Fabrication Simulation

14:332:468 Microelectronics Processing

by

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Abstract – MOSFET scaling is a necessary process which results in more devices being able to fit on the wafer surface. Reducing the size of the devices results in its own set of problems. The properties of semiconductors lead to different behavior by FETs with short channels as opposed to those with long channels. We set out to overcome the challenges imposed by the aforementioned Short Channel Effects (SCE). Our simulation was done in TSUPREM4 and Medici simulation environments. The performance standards we aimed to achieve were stipulated by the ITRS.

Background

Device considerations need to be changed purely because of short channel effects. These effects have an unwanted reaction, altering the desired device.

Figure 1a and 1b depicts what an Id vs Vds curve looks like normally and under SCE respectively.
At short gate lengths, devices suffer from hot carrier effects, punch-through, lack of pinch off region, threshold voltage shift, and band to band tunneling currents. Hot carrier effects can be broken down even further into sub-categories beginning with oxide charging. Oxide charging, or charge injection and trapping in the oxide, occurs in all devices, regardless long or short. Channel carriers and drain carriers entering the drain depletion region from the substrate, gain enough energy to penetrate the oxide layer and enter into the oxide itself. Charge begins to buildup within the oxide which can cause significant changes in Vt and gm and also affect the usefulness of the device since the charge increases over time. Velocity overshoot and ballistic transport become a concern when the channel is much greater than the average distance between the scattering of the carriers travelling between the source and the drain. Substrate punch-through occurs when the source and drain depletion regions envelope and become one. This is not a concern in long devices but in small ones it is very important to address. As can be seen from Fig.1b, there is a lack of a pinch off region because of SCE which entails the device never remains in the desired constant Id value when in saturation. The shift in threshold voltage is one of the biggest, if not, the main concern since it will skyrocket due to the nature of the device. As the device gets smaller, it becomes more complicated to keep Vt at the desired level. Tunneling currents will generate unwanted leakage current and will hinder performance of the device. In the next section, the measures taken to counter these problems will be discussed.
**Process**

Create Bulk
- Initialize \(<100>\) Boron 1E15
- Epitaxy 20nm, 30s, 700C, In-Situ doping 1E19
- Epitaxy 50nm, 90s, 700C
- Diffusion 6.9 mins, 850C Dry O2
- Etch 2.2nm of Oxide

Form Gate
- Deposit Polysilicon 60nm
- Deposit Nitride 10nm

Expose ‘Gate’ Mask and Etch
- Etch Nitride 10nm
- Etch Polysilicon 60nm
- Etch Oxide 3.3nm

Initial Spacer Formation
- Deposit Nitride 6nm
- Etch Nitride 6nm

Source/Drain Doping (Solid Source Diffusion Method)
- Deposit Polysilicon 1um, Phosphorous dose = 1E20
- Diffusion 12s, 700C, Nitrogen ambient
- Etch all Polysilicon

Second Stage Spacer Formation
- Deposit Nitride 5nm
- Etch Nitride 5nm

Drive in Source/Drain Dopants
- Diffusion 6s, 700C, Nitrogen ambient

Full Salicidation Process
- Deposit Nickel 10nm
- Diffusion 3.6s, 350C, Nitrogen ambient
- Etch all excess Nickel
- Diffusion 140mins, 300C, Nitrogen ambient
- Etch all Nickel

Form Metal Contacts

- Expose ‘contact’ mask
- Deposit Aluminum 100um
- Expose ‘metal’ mask
- Etch all Aluminum

Figure 2 depicts the completed structure. Blue=Phosphorous, Pink = Boron, White=Nitride, Yellow=bulk, Green=Polysilicon, NiSi2, Red = Aluminum.
Process Description

First we initialize the bulk on top of which the device will be constructed. We initialized a $<100>$ orientation Silicon bulk with Boron background doping at $1\text{E}15$. Then an epitaxial layer of thickness 20nm was grown with in-situ Boron doping with a dose of $1\text{E}19$. This forms a barrier layer preventing dopants from the S/D process getting too far into the bulk, ensuring a shallow junction. This layer of doping also counters the punch-through effect that arises in short channel devices. Then a second epitaxial layer is formed of thickness 50nm. A diffusion step is performed for 6.9 mins at 850C to round out the initialization process. This diffusion process grows the gate oxide and further disperses the dopants in the bulk. We etch away 2.2nm of Oxide from the top layer so we have a thinner gate oxide that conforms ITRS standards. We now have a bulk to construct our device on.

The next process is the formation of the gate by the standard methods. First we deposit a 60nm layer of Polysilicon, followed by a 10nm layer of Nitride. After depositing photoresist and exposing the gate mask, we etch away the excess Nitride, Polysilicon, and Oxide. This results in a simple poly gate on top of an oxide, and no additional structures on the bulk.

The spacer formation is broken into two steps. The first step is to deposit 6nm of nitride, and then etching away all of it. This leaves a 6nm thick spacer on the side of the Polysilicon gate. Before the second spacer is formed, we perform the Source and Drain junctions as outlined in the next step. By forming a second layer of spacer after creating the n-wells, we ensure that a section of the formed S/D junction is below the spacer. This reduces the influence of hot carrier of effects and DIBL.
As mentioned earlier, after the first layer of nitride is formed, we perform the Source/Drain doping for the device. The process used is called solid source diffusion. This is done by depositing one micron of Polysilicon that has been doped by Phosphorous at a dose of 1E20. A short diffusion step for 12 seconds at 700C in Nitrogen releases dopants into the bulk. After the diffusion we etch away all the doped Polysilicon. After the second spacer, we again drive in the dopants into the bulk. This is achieved by performing diffusion for 6 seconds at 700C in a Nitrogen ambient.

The next step is to form a Salicide layer on top of the source drain regions. The Salicide reduces the total resistance at the contact regions and offers minimal electromigration. We form the FUSI(Fully Silicided) layer by first depositing Nickel on the bulk. Then we carry out diffusion for 3.6 seconds at 350C in Nitrogen. Then all the excess Nickel is etched away. To fully silicide the layer, we run diffusion again for 140 minutes at 300C in Nitrogen. With the FUSI layer formed, we deposit 100nm of oxide. Using the relevant masks, we etch a hole above contacts and deposit Aluminum to complete the metallization process. The device is now complete and ready for export into Medici.
Results

First we examine the distribution of dopants at various points in the device.

Figure 3a and 3b show the dopant distribution under the gate and under the Nitride spacer respectively.

Figure 4a plots the dopant distribution under the contact region. Figure 4b plots the dopant distribution horizontally along a line approximately .4nm below the gate/bulk contact point.
Figure 5a and 5b plot the doping distribution along lines 5nm and 10nm below the gate/bulk contact point respectively.

Having observed the dopant distribution in the device, we move on to determining I-V characteristics.

Figure 6a and 6b show the Id-Vgs relation in the saturation and linear region respectively.
Figure 7 shows the standard Id-Vds curve at various values of Vgs.

Table 1 compares the results of our simulation and properties of the device with those stipulated by the ITRS specifications.

<table>
<thead>
<tr>
<th></th>
<th>ITRS Specification</th>
<th>Experimental Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lg (gate length)</td>
<td>22nm</td>
<td>20nm</td>
</tr>
<tr>
<td>tox (EOT)</td>
<td>1nm</td>
<td>1nm</td>
</tr>
<tr>
<td>xj</td>
<td>10nm</td>
<td>~10nm</td>
</tr>
<tr>
<td>DIBL</td>
<td>&lt;100nm</td>
<td>55.3mV</td>
</tr>
<tr>
<td>STS</td>
<td>&lt;100nm</td>
<td>87.08mV</td>
</tr>
<tr>
<td>Vtsat</td>
<td>650mV</td>
<td>247mV</td>
</tr>
<tr>
<td>Vtlin</td>
<td>n/a</td>
<td>302mV</td>
</tr>
</tbody>
</table>

Table 1 compares the results of our simulation and properties of the device with those stipulated by the ITRS specifications.
Conclusion

The short channel effects mentioned earlier were countered by the steps mentioned throughout the process flow. These steps successfully suppressed the short channel effects we expected to encounter during the design process. There were many complications we had to counter, such as the formation of the silicide, achieving shallow junction depth, and not meeting ITRS standards. Ultimately, after several iterations of changes made in our process, we overcame the aforementioned hindrances. The device performs accurately according to the expectations of the ITRS and functions properly as a Low Standby Power NMOS.
References


**Source Code**

**Mask File:**

TL1 0100

/ Capstone mask definition.

1e3
0 0200
4
Field 1
0 0025
Poly 1
0 0010
Contact 2
0 0060
0100 0200
Metal 1
0000 0045

**TSUPREM-4 Code:**

define lgate .02
define contactdistance .05
define contactwidth .05
define boundary .2
define aligntol .03
mesh grid.fac=1.0
MASK IN.FILE=mask.tl1 PRINT GRID="Field,Poly,Contact,Metal"

INITIALIZE <100> BORON=1E15

EPITAXY THICKNES=.02 TIME=.5 TEMP=700 BORON=1E19

EPITAXY THICKNES=.05 TIME=1.5 TEMP=700

DIFFUSION TIME=6.9 TEMP=850 DRY

ETCH OXIDE THICKNES = .0022

$Gate stack formation

DEPOSIT POLYSILICON THICKNES=.06

DEPOSIT NITRIDE THICKNES=.01

$Gate etch

DEPOSIT PHOTORESIST THICKNES=1

EXPOSE MASK=Poly

DEVELOP

ETCH NITRIDE THICKNES=.01 DRY

ETCH POLYSILICON THICKNES=.06 DRY

ETCH OXIDE THICKNES=.0033 DRY

ETCH PHOTORESIST ALL

$First spacer formation

DEPOSIT NITRIDE THICKNES=.006

ETCH NITRIDE THICKNES=.006 DRY

$S/D doping

DEPOSIT POLYSILICON THICKNES=1 PHOSPHORUS=1E20

DIFFUSION TIME=.2 TEMP=700 INERT

ETCH POLYSILICON DRY
$Second Spacer formation
DEPOSIT NITRIDE THICKNES=.005
ETCH NITRIDE THICKNES=.005 DRY

$S/D drive in
DIFFUSION TIME=.1 TEMP=700 INERT

$Salicidation
DEPOSIT MAT=NICKEL THICKNES=.01
DIFFUSION TEMP=350 TIME=.06 INERT
ETCH MAT=NICKEL DRY

$FUSI formation
ETCH NITRIDE THICKNES=.01 DRY
METHOD PD.FERMI
DIFFUSION TIME=140 TEMP=300 INERT
ETCH MAT=NICKEL DRY

$Contact hole
DEPOSIT OXIDE THICKNES=.1
DEPOSIT PHOTORESIST THICKNES=1
EXPOSE MASK=Contact
DEVELOP
ETCH OXIDE DRY
ETCH PHOTORESIST ALL

$Metallization
DEPOSIT ALUMINUM THICKNES=.1
DEPOSIT PHOTORESIST NEGATIVE THICKNES=1
EXPOSE MASK=Metal
DEVELOP
ETCH ALUMINUM THICKNES=.1 DRY
ETCH PHOTORESIST ALL
STRUCTURE REFLECT LEFT

electrode name=gate  x=0
electrode name=drain  x=(@{lgate}/2)+@{contactdistance}+(@{contactwidth}/2)
electrode name=source x=-(@{lgate}/2)-@{contactdistance}-(@{contactwidth}/2)
electrode name=substrate bottom

SELECT Z=LOG10(BORON)
PLOT.2D  Y.MAX=.2  Y.MIN=-.4 X.MAX=.2
COLOR SILICON COLOR=7
COLOR OXIDE COLOR=5
COLOR POLY COLOR=3
COLOR ALUM COLOR=2
COLOR MAT=NISI2 COLOR=3
COLOR MAT=NICKEL COLOR=7
FOREACH X (15 TO 20 STEP 1)
CONTOUR VALUE=X LINE=5 COLOR=6
END

SELECT Z=LOG10(PHOSPHORUS)
FOREACH X (18 TO 21 STEP 1)
CONTOUR VALUE=X LINE=2 COLOR=4
END
SAVEFILE MEDICI OUT.FILE=CAPS.STR

Medici Code:

mesh in.file=CAPS.STR TSUPREM4 POLY.ELEC

COMMENT Id vs Vg plot

SYMB NEWTON CARRIERS=1 ELECTRONS

SOLVE V(drain)=1

SOLVE V(gate)=.2 ELEC=gate VSTEP=.1 NSTEP=8

PLOT.1D Y.AXIS=I(drain) X.AXIS=V(gate) POINTS Y.LOGARI COLOR=2

COMMENT Id vs Vd plot

SYMB CARRIERS=0

METHOD ICCG DAMPED

SOLVE V(gate)=1

SYMB NEWTON CARRIERS=1 ELECTRON

SOLVE V(drain)=0.0 ELEC=drain VSTEP=.1 NSTEP=10

PLOT.1D Y.AXIS=I(drain) X.AXIS=V(drain) TOP=4E-3 BOTTOM=.1E-5 ^CLEAR COLOR=2

LABEL LABEL="Vgs=1V" X=.8 Y=2E-4

COMMENT STRUCTURE PLOT

PLOT.2D X.MAX=.2 Y.MAX=.4 FILL BOUND

CONTOUR DOPING LOG MIN=16 MAX=20 COLOR=2 DEL=.5

CONTOUR DOPING LOG MIN=-16 MAX=-15 DEL=.5 COLOR=1 LINE=2